WHAT IS CLAIMED IS:

1. An output stage of an amplifier circuit having an input amplifier stage, said output stage comprising:

circuitry operable to source an output current to an external load;

circuitry coupled to said sourcing circuitry and operable to sink current from the external load, said sourcing circuitry and said sinking circuitry having a common output node;

circuitry responsive to the input amplifier stage, coupled to said sinking circuitry and operable to approximately mirror the current in said sinking circuitry;

a current balancing circuit responsive to said mirroring circuitry and coupled to control said sourcing circuitry;

said mirroring circuitry operable to draw current from said balancing circuit in response to a first predetermined output from the input amplifier stage such that said balancing circuit causes an insignificant current to flow in said sourcing circuitry and said mirroring circuit operable to cause said sinking circuit to sink a significant current from the external load; and

said mirroring circuitry operable to draw an insignificant current from said balancing circuit in response to a second predetermined output from the input amplifier stage such that said balancing circuit causes a significant current to flow in said sourcing circuitry.

2. The output stage of Claim 1, wherein said sinking circuitry comprises an NPN bipolar junction transistor and said sourcing circuitry comprises a PNP bipolar junction transistor.

3. The output stage of Claim 1, wherein said sourcing circuitry comprises:

a PNP bipolar junction transistor; and

an NPN bipolar junction transistor having a base coupled to an emitter of said PNP transistor to form a Darlington pair.

4. The output stage of Claim 1, wherein said current balancing circuit comprises:

first and second current sources;

first and second transistors;

said transistors coupled to form a current mirror;

a collector of said first transistor coupled to a base of said first transistor, a base of said second transistor, said first current source and said mirroring circuitry; and

a collector of said second transistor coupled to said sourcing circuitry and said second current source such that the current in said first transistor is mirrored in said second transistor to control said sourcing circuitry.

5. The output stage of Claim 1, wherein said current balancing circuit comprises:

first and second circuit sources;

first and second transistors;

said transistors coupled to form a current mirror;

a diode coupled between an emitter of said transistors and a ground potential;

a collector of said first transistor coupled to a base of said first transistor, a base of said second transistor, said first current source and said mirroring circuitry; and

a collector of said second transistor coupled to said sourcing circuitry and said second current source such that the current in said first transistor is mirrored in said second transistor to control said sourcing circuitry.

6. The output stage of Claim 1, wherein said mirroring circuitry comprises an NPN bipolar junction transistor having a resistor coupled between an emitter of said transistor and a ground potential, said resistor operable to control the rate of increase of current through said mirroring circuitry as said output stage performs a sinking operation.

7. The output stage of Claim 1, wherein said mirroring circuitry comprises an NPN bipolar junction transistor, and further comprising a voltage clamp coupled to said transistor for establishing a predetermined lower voltage limit to prevent said transistor from interfering with said sinking circuitry during a sinking operation.

8. The output stage of Claim 1, wherein said mirroring circuitry comprises an NPN bipolar junction transistor, said output stage further comprising:

a voltage clamp coupled to said mirroring circuitry for establishing a predetermined lower voltage limit to prevent said mirroring circuitry from interfering with said sinking circuitry during a sinking operation; and

a resistor coupled between an emitter of said transistor of said mirroring circuitry and a ground potential, said resistor operable to control the rate of increase of current through said mirroring circuitry.

9. The output stage of Claim 1, and further comprising a voltage clamp for establishing a predetermined lower voltage limit for said mirroring circuitry, said clamp comprising:

first and second diodes coupled in series between a current source and ground; and

an NPN bipolar junction transistor having a base coupled to an output of said current source and an emitter coupled to said mirroring circuitry.

10. The output stage of Claim 1, and further comprising a voltage clamp for establishing a predetermined lower voltage limit for said mirroring circuitry, said clamp comprising:

first, second and third diodes coupled in series between a current source and ground; and

a Darlington pair of NPN bipolar junction transistors having a base coupled to an output of said current source and an emitter coupled to said mirroring circuitry.

11. The output stage of Claim 1, wherein said mirroring circuitry comprises first and second NPN bipolar junction transistors coupled to form a Darlington pair.

12. An operational amplifier, comprising:

an input amplifier stage having an output;

a bipolar junction transistor for sourcing current to an external load;

a bipolar junction transistor for sinking current from the external load, a collector of said sourcing transistor coupled to a collector of said sinking transistor to form a common output node;

a mirroring bipolar junction transistor having a base coupled to a base of said sinking transistor such that current and said sinking transistor approximately mirrors current in said mirroring transistor;

a current balancing circuit responsive to said mirroring transistor and coupled to control said sourcing transistor;

said mirroring transistor operable to draw current from said balancing circuit in response to a first predetermined output from the input amplifier stage such that said balancing circuit causes an insignificant current to flow in said sourcing transistor and said mirroring circuit operable to cause said sinking transistor to sink a significant current from the external load; and

said mirroring transistor operable to draw an insignificant current from said balancing circuit in response to a second predetermined output from the input amplifier stage such that said balancing circuit causes a significant current to flow in said sourcing transistor.

13. The amplifier of Claim 12, wherein said sourcing transistor comprises a PNP bipolar junction transistor and said sinking and mirroring transistors comprise NPN bipolar junction transistors.

14. The amplifier of Claim 12, wherein said sourcing transistor comprises:

a PNP bipolar junction transistor; and

an NPN bipolar junction transistor having a base coupled to an emitter of said PNP transistor to form a Darlington pair.

15. The amplifier of Claim 12, wherein said current balancing circuit comprises:

first and second current sources;

first and second transistors;

said transistors coupled to form a current mirror;

a collector of said first transistor coupled to a base of said first transistor, a base of said second transistor, said first current source and said mirroring transistor; and

a collector of said second transistor coupled to said sourcing transistor and said second current source such that the current in said first transistor is mirrored in said second transistor to control said sourcing transistor.

16. The amplifier of Claim 12, wherein said current balancing circuit comprises:

first and second current sources;

first and second transistors;

said transistors coupled to form a current mirror;

a diode coupled between an emitter of said transistors and a ground potential;

a collector of said first transistor coupled to a base of said first transistor, a base of said second transistor, said first current source and said mirroring transistor; and

a collector of said second transistor coupled to said sourcing transistor and said second current source such that the current in said first transistor is mirrored in said second transistor to control said sourcing transistor.

17. The amplifier of Claim 12, wherein said mirroring transistor comprises an NPN bipolar junction transistor, said amplifier further comprising:

a voltage clamp coupled to said mirroring transistor for establishing a predetermined lower voltage limit to prevent said mirroring transistor from interfering with said sinking transistor during a sinking operation; and

a resistor coupled between an emitter of said mirroring transistor and a ground potential, said resistor operable to control the rate of increase of current through said mirroring transistor.

18. The amplifier of Claim 12, and further comprising a voltage clamp for establishing a predetermined lower voltage limit for said mirroring transistor, said clamp comprising:

first and second diodes coupled in series between a current source and a ground potential; and

an NPN bipolar junction transistor having a base coupled to an output of said current source and an emitter coupled to a collector of said mirroring transistor.

19. A method for controlling an output current of an amplifier circuit having sourcing and sinking circuits coupled to a common output node, said method comprising the steps of:

generating a control output signal from an input amplifier stage of the amplifier circuit in response to an input to the amplifier circuit;

providing the control signal to a mirror circuit that mirrors the current and to the sinking circuit;

drawing current from a current balancing circuit in response to a first predetermined output of the amplifier stage such that the balancing circuit causes an insignificant current to flow in the sourcing circuit and significant current flow in the sinking circuit; and

drawing an insignificant current from said balancing circuit in response to a second predetermined output from the amplifier stage such that the balancing circuit causes a significant current to flow in said sourcing circuitry.

20. The method of Claim 19, and further comprising the steps of:

establishing a predetermined lower voltage limit at the collector of a transistor of the mirror circuit with a voltage clamp; and

limiting the high current range of the transistor of the mirror circuit by a resistor coupled to the emitter of the transistor such that the transistor does not saturate during a sinking operation and divert current from the sinking circuit.